ponents and structures of the TFT array substrate are similar to those related to the fifth preferred embodiment except that the passivation layer **70** is absent, and the black matrix **90** serves the function of the passivation layer **70**. Therefore, the separate step of forming the passivation layer **70** is eliminated in this preferred embodiment.

The black matrix **90** is formed with a photosensitive material containing black pigments. In the etching process based on the third mask, the photosensitive matrix layer is itself exposed to light through the third mask without forming the photosensitive film PR, and developed to thereby form the black matrix pattern **90**. In the subsequent processing steps, the black matrix pattern **90** serves the function of the photoresist pattern PR.

In the above structure, the number of the processing steps can be reduced.

Tenth Preferred Embodiment

FIGS. **48**A and **48**B illustrate the structure of a TFT array substrate according to a tenth preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the TFT array substrate are similar to those related to the ninth preferred embodiment except that the gate insulating layer **30** has a different pattern. That is, the portion of the gate insulating layer at the pixel area between the neighboring data lines is removed such that it has the same shape as that of the semiconductor pattern **40**. Therefore, the color filter **100** is positioned directly over the substrate **10** and the gate line **22**. The width of the removed portion of the gate insulating layer at the pixel area should be 1 μ or more. That is, the opening width of the semiconductor layer **40** should reach 1 μ or more. The opening prevents the currents from leaking between the neighboring data lines **62** via the semiconductor layer **40**.

In the method of fabricating the TFT array substrate according to the tenth preferred embodiment, the processing steps are similar to those related to the ninth preferred embodiment except that a usual mask with only a transparent portion and an opaque portion is used for the third mask. That is, the transparent portion of the mask corresponds to the portion of the target film to be removed, while the opaque portion corresponds to the portion of the target film to remain.

When the photosensitive black matrix pattern **90** is formed by using the usual mask, and the underlying semiconductor layer and gate insulating layer are etched by using the photosensitive black matrix pattern **90** as a photoresist pattern PR, exposing the portions of the substrate **10** and the gate line **21** between the neighboring data lines **62** to the outside, and the contact windows **71** to **73** are also formed.

Thereafter, a color filter **100** as well as a pixel electrode **82**, a supplemental gate pad **84** and a supplemental data pad **86** are formed in the similar way as in the ninth preferred embodiment. The color filter **100** completely covers the exposed portion of the gate line **22** to insulate the gate line **22** from the pixel electrode **82**.

The above mentioned structure can reduce, the number of processing steps even with the usual mask having only transparent and opaque portions.

As described above, the TFT array substrate of the present invention can be fabricated with simplified processing steps while achieving good performance characteristics.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

What is claimed is:

1. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a first contact window exposing the gate pad, and an opening portion partially exposing the insulating substrate;

a semiconductor pattern formed on the gate insulating layer;

a contact pattern formed on the semiconductor pattern;

a data line assembly formed on the contact pattern with substantially the same outline as the contact pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrode while being separated from the source electrodes;

a passivation layer formed on the data line assembly with the same outline as the semiconductor pattern except at portions of a second contact window exposing the data pad and a third contact window exposing the drain electrode;

a pixel electrode formed at a pixel area defined by the neighboring gate and data lines, the pixel electrode being electrically connected to the drain electrode through the third contact window while partially contacting the gate insulating layer; and

subsidiary gate and data pads contacting the gate and data pads, respectively.

2. The thin film transistor array substrate of claim **1** wherein the opening portion exposes the substrate between the pixel electrode and the neighboring data line.

3. The thin film transistor array substrate of claim **1** wherein the third contact window exposing the drain electrode is extended such that the borderline of the drain electrode is exposed to the outside.

4. A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes;

a second insulating layer formed on the data line assembly with the same outline as the semiconductor pattern, the second insulating layer having a second contact window exposing the gate pad through the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

5. The thin film transistor array substrate of claim **4** further comprising a contact layer formed between the semiconductor pattern and the data line assembly with the same outline as the data line assembly.

6. The thin film transistor array substrate of claim **4** further comprising supplemental gate pads and supplemental data pads covering the gate pad and the data pad, respectively.

7. The thin film transistor array substrate of claim **4** further comprising a photo-interceptive organic pattern formed between the data line assembly and the overlying passivation layer.

8. The thin film transistor array substrate of claim **7** wherein the photo-interceptive pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

9. The thin film transistor array substrate of claim **4** wherein the second insulating layer is formed of a photo-interceptive organic layer.

10. The thin film transistor array substrate of claim **9** wherein the first insulating layer has the same outline as the semiconductor pattern.

11. The thin film transistor array substrate of claim **10** wherein the opening width of the semiconductor pattern between the neighboring data lines is 1 μ or more.

12. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes, the data line assembly substantially having the same outline as the semiconductor pattern except the portion placed between the source electrode and the drain electrode;

a second insulating layer formed on the data line assembly, the second insulating layer having a second contact window exposing the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed on the passivation layer at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

13. The thin film transistor array substrate of claim **12** further comprising a contact layer formed between the semiconductor pattern and the data line assembly substantially with the same outline as the data line assembly.

14. The thin film transistor array substrate of claim **12** further comprising supplemental gate pads and supplemental data pads covering the gate pads and the data pads, respectively.

15. The thin film transistor array substrate of claim **12** further comprising a photo-interceptive organic pattern formed on the passivation layer over the data line assembly and the gate line assembly.

16. The thin film transistor array substrate of claim **15** wherein the photo-interceptive organic pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

17. The thin film transistor array substrate of claim **12** wherein the second insulating layer is formed with a photo-interceptive organic layer.

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